Register No.:

301

April 2023

Time – Three hours
(Maximum Marks: 100)

N.B. 1. Answer all questions under Part-A. Each question carries 3 marks.
2. Answer all the questions either (A) or (B) in Part-B. Each question carries 14 marks.

PART – A

1. Define the parameters of SVRR and slew rate of op-amp.
2. Draw the block diagram of integrator.
3. Define weighted resistor D/A converter.
4. Define ramp type ADC.
5. Define universal logic gates. Give examples.
6. Define signed binary numbers.
7. Define 1 to 4 DEMUX.
8. Write about mod-N counter.
9. State the different types of memory.
10. Define non volatile memory.

PART – B

11 A) (i) Explain CMRR. (7)
(ii) Explain op-amp as non-inverting amplifier. (7)

(OR)

B) Explain about zero crossing detector using op-amp.

[Turn over...

12 A) With the diagram explain successive approximation ADC.

(OR)

B) (i) Explain about IC 79XX regulators. (7)
(ii) Draw the functional block diagram of IC 555. (7)

13 A) (i) Convert the decimal number 73.81 to its equivalent octal, hexadecimal and binary numbers. (10)
(ii) State De-Morgan's theorem. (4)

(OR)

B) Construct AND, OR, NOT, NAND and EX-OR gates by using only NOR gates.

14 A) With the logic diagram and truth table explain JKMS flip flop.

(OR)

B) With the logic diagram and truth table explain SR-flip flop.

15 A) Explain how read and write operations are performed in memory.

(OR)

B) (i) Explain briefly about SDRAM. (7)
(ii) Explain briefly about DDR RAM. (7)
