608 Register No.:

April 2024

Time – Three hours
(Maximum Marks: 100)

[N.B. 1. Answer all questions under Part-A. Each question carries 3 marks.

2. Answer all the questions either (A) or (B) in Part-B. Each question carries 14 marks.]

PART – A

1. Draw NAND gate using NMOS.
2. Define simulation. Mention its types.
3. Write the syntax for signal assignment statement.
4. Give an example for case statement.
5. Draw the block diagram and truth table for 1 to 4 demultiplexer.
6. Draw the circuit diagram for single bit comparator.
7. Draw the diagram for 3-bit up/down counter.
8. Compare D flipflop and T flipflop.
9. Expand CPLD, FPGA, ASIC.
10. Compare PLA and PAL.

[Turn over.....

PART – B

11. (a) Implement the function Y=A+BC using CMOS.

(Or)

(b) What are the different levels of abstractions in VLSI design? Explain.

12. (a) Explain the different types of modelling in HDL.

(Or)

(b) Write a VHDL code for Logic gates NOR, OR.

13. (a) Write a VHDL program for 2 to 4 decoder with diagram.

(Or)

(b) Draw and explain the block diagram, circuit diagram and truth table for four bit arithmetic adder.

14. (a) Explain about ring counter with diagram.

(Or)

(b) Write a VHDL program for Johnson counter.

15. (a) Explain design steps in ASIC.

(Or)

(b) Implement the function $y=\sum(0,2,3,4,5,7)$ using PLA.
